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April N. Williams
April N. Williams

09/980974
JC13 Rec'd PCT/PTO 26 OCT 2001

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Jensen et al. Group Art Unit: Not Assigned

Serial No.: Not Assigned Examiner: Not Assigned

Filed: Herewith Docket No.: 1406/24

For: METHOD AND DEVICE OR BRANCHING DURING THE PROCESSING OF A PROGRAM BY A PROCESSOR

* *

PRELIMINARY AMENDMENT

Honorable Commissioner for Patents
BOX PCT
Washington, D.C. 20231

Dear Sir:

Kindly amend the subject application as follows:

IN THE SPECIFICATION:

Please insert the paragraph heading on page 1 of the English translation of the Annex to Form PCT/IPEA/409, after the title and before the first full paragraph, as follows:

--Technical Field --.

Please insert the paragraph heading on page 1 of the English translation of the Annex to Form PCT/IPEA/409, before the second full paragraph, as follows:

--Background Art --.

Please insert the paragraph heading on page 2 of the English translation of the Annex to Form PCT/IPEA/409, before the first full paragraph, as follows:

--Summary of the Invention--.

Please insert the paragraph heading on page 3 of the English translation of the Annex to Form PCT/IPEA/409, before the fifth full paragraph, as follows:

--Brief Description of the Drawings--.

Please insert the paragraph heading on page 4 of the English translation of the Annex to Form PCT/IPEA/409, before the second full paragraph, as follows:

--Detailed Description of the Invention--.

IN THE CLAIMS:

Please delete the paragraph heading on page 9 of the English translation of the annex to Form PCT/IPEA/409, line 1, and insert in place thereof the paragraph heading as follows:

--CLAIMS--

Please insert the paragraph heading on page 9 of the English translation of the annex to Form PCT/IPEA/409, before claim 1, the following:

-- What is claimed is: --.

Please amend claims 1-8 as follows:

1. (Amended) A method for branching when a program is executed by a processor, where the program is stored in a program memory, and a variable memory and a table memory for storing fixed values are provided, the processor executing the following steps:

a) a first memory cell in the variable memory is addressed,

b) a second memory cell in the variable memory is addressed on the basis of the content of the first memory cell, addressed in step a), and further parameters,

c) a memory cell in the table memory is addressed on the basis of the content of the second memory cell, addressed in step b), and

d) execution branches to a program address which is stored in that memory cell in the table memory which was addressed in step c).

2. (Amended) The method as claimed in claim 1, wherein in step b), the second memory cell in the variable memory is addressed by the result of an instruction which processes the content of the first memory cell in the variable memory and further parameters.

3. (Amended) The method as claimed in claim 1, wherein the variable memory is addressed using a first bit length a, and the table memory is addressed using a second bit length b, the first bit length a and the second bit length b being of different size.

4. (Amended) An apparatus for carrying out the method as claimed in claim 1, where

the program memory is connected to the processor by means of a bidirectional bus,

an addressing unit is provided which receives first addresses from the processor via a bus and converts the first addresses into second addresses, and thus uses a bus to address the variable memory, which can be read by the processor via a bus, and

the table memory is connected to the processor by means of a bidirectional bus.

5. (Amended) The apparatus as claimed in claim 4, wherein a device is provided which receives data from the variable memory via a bus and receives data

from the processor via a bus, and uses the received data to calculate an address for addressing the variable memory via a bus.

6. (Amended) The apparatus as claimed in claim 4, wherein the variable memory is a read/write memory.

7. (Amended) The apparatus as claimed in claim 4, wherein the table memory is a read/write memory.

8. (Amended) The apparatus as claimed in claim 4, wherein the processor is in the form of an I/O processor for protocol processing.

REMARKS

The amendments to the specification as set forth above are intended to clarify and set apart the various sections of the subject application.

The amendments to the claims as set forth above are intended to remove all multiple dependent claims from the subject application and to more particularly point out and distinctly claim the subject invention.

Attached hereto is a marked-up version of the specification and claims 1-8, which illustrates all of the changes made to the specification and claims pursuant to 37 CFR §1.121. The attached page is captioned "**Version With Markings To Show Changes Made**". Deleted language is bracketed and added language is underlined.

The Commissioner is hereby authorized to charge any deficiencies or credit any overpayments in connection with the filing of this correspondence to Deposit Account No. **50-0426**.

Respectfully submitted,

JENKINS & WILSON, P.A.

Date: 10-26-01

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25297
PATENT TRADEMARK OFFICE

1406/24 REJ/lsg

Serial No.: Not yet assigned

Version With Markings To Show Changes Made

IN THE SPECIFICATION:

The paragraph heading has been inserted on page 1 of the English translation of the Annex to Form PCT/IPEA/409, before the first full paragraph, as follows:

Technical Field

The paragraph heading has been inserted on page 1 of the English translation of the Annex to Form PCT/IPEA/409, before the second full paragraph, as follows:

Background Art

The paragraph heading has been inserted on page 2 of the English translation of the Annex to Form PCT/IPEA/409, before the first full paragraph, as follows:

Summary of the Invention

The paragraph heading has been inserted on page 3 of the English translation of the Annex to Form PCT/IPEA/409, before the fifth full paragraph, as follows:

Brief Description of the Drawings

The paragraph heading has been inserted on page 4 of the English translation of the Annex to Form PCT/IPEA/409, before the second full paragraph, as follows:

Detailed Description of the Invention

IN THE CLAIMS:

The paragraph heading "Patent Claims" on page 1 of the English translation of the Annex to Form PCT/IPEA/409 has been deleted and the paragraph heading has been inserted in place thereof as follows:

CLAIMS

The paragraph heading has been inserted on page 1 of the English translation of the Annex to Form PCT/IPEA/409, before claim 1, as follows:

What is claimed is:

1. (Amended) A method for branching when a program is executed by a processor [(100)], where the program is stored in a program memory [(5)], and a variable memory [(6)] and a table memory [(7)] for storing fixed values are provided, the processor [(100)] executing the following steps:

a) a first memory cell [(12)] in the variable memory [(6)] is addressed [(1)],

b) a second memory cell [(13)] in the variable memory is addressed [(2)] on the basis of the content of the first memory cell [(12)], addressed in step a), and further parameters [(11)],

c) a memory cell [(14)] in the table memory [(7)] is addressed [(3)] on the basis of the content of the second memory cell [(13)], addressed in step b), and

d) execution branches to a program address [(15)] which is stored in that memory cell [(14)] in the table memory [(7)] which was addressed in step c).

2. (Amended) The method as claimed in claim 1, [characterized in that] wherein in step b), the second memory cell [(13)] in the variable memory [(6)] is addressed by the result of an instruction [(10)] which processes the content of the first memory cell [(12)] in the variable memory [(6)] and further parameters [(11)].

3. (Amended) The method as claimed in claim 1 [or 2, characterized in that], wherein the variable memory [(6)] is addressed [(1)] using a first bit length a, and the table memory [(7)] is addressed [(3)] using a second bit length b, the first bit length a and the second bit length b being of different size.

4. (Amended) An apparatus for carrying out the method as claimed in claim 1, where

the program memory [(5)] is connected to the processor [(100)] by means of a bidirectional bus [(103)],

an addressing unit [(101)] is provided which receives first addresses from the processor [(100)] via a bus [(104)] and converts the first addresses into second addresses, and thus uses a bus [(105)] to address the variable memory [(6)], which can be read by the processor [(100)] via a bus [(109)], and

the table memory [(7)] is connected to the processor [(100)] by means of a bidirectional bus [(110)].

5. (Amended) The apparatus as claimed in claim 4, [characterized in that] wherein a device [(102)] is provided which receives data from the variable memory [(6)] via a bus [(106)] and receives data from the processor [(100)] via a bus [(106)], and uses the received data to calculate an address for addressing the variable memory [(6)] via a bus [(107)].

6. (Amended) The apparatus as claimed in claim [4 or 5, characterized in that] 4, wherein the variable memory [(5)] is a read/write memory.

7. (Amended) The apparatus as claimed in claim [4, 5 or 6, characterized in that] 4, wherein the table memory [(7)] is a read/write memory.

8. (Amended) The apparatus as claimed in [one of Claims 4 to 7, characterized in that] claim 4, wherein the processor [(100)] is in the form of an I/O processor for protocol processing.

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Description

Method and apparatus for branching when a program is executed by a processor

The invention relates to a method for branching when a program is executed by a processor and to an apparatus for carrying out the method.

WO 96/08763 discloses a method for branching when a program is executed by a processor, where the processor executes an indirect instruction in a double jump register by using the content of a designated pointer register to determine the address of a procedure which is to be executed as an index to a procedure address table.

Instructions for branching during program execution by a processor - also referred to as jump instructions - are divided up into indirect and direct jump instructions.

In this context, indirect jump instructions calculate the destination address of the program branch operation or of the jump indirectly using the content of an "index register". The value stored in the index register can be varied during program execution, so that the jump destination can be programmed within particular ranges. A drawback in this case, however, is that indirect jump instructions are executed in single stages (a stage for calculating the jump or branch destination), and the jump or the branch operation can be executed in two stages only under complex conditions using a large number of instructions. The advantage of two-stage execution is simple reprogrammability and adaptability of jump or branch destinations as the jump is processed.

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The invention is therefore based on the object of providing a method for branching when a program is executed by a processor, and an appropriate apparatus for carrying out the method, which permits two-stage program branching using variable indirect addressing.

This object is achieved by a method having the features of claim 1 and by an apparatus having the features of claim 4. Preferred embodiments of the invention are the subject matter of the subclaims.

According to the invention, a method for branching when a program is executed by a processor, where the program is stored in a program memory, and a variable memory and a table memory are provided, has the following steps executed by the processor:

a) a first memory cell in the variable memory is addressed,

b) a second memory cell in the variable memory is addressed on the basis of the content of the first memory cell, addressed in step a), and further parameters,

c) a memory cell in the table memory is addressed on the basis of the content of the second memory cell, addressed in step b), and

d) execution branches to a program address which is stored in that memory cell in the table memory which was addressed in step c).

Advantageously, the two-stage branch operation (first stage: step a) and b), second stage: step c)) allows variable indirect addressing of the jump or branch destination. In this case, the variable indirect addressing can be influenced by further parameters in step b).

Preferably, in step b), the second memory cell in the variable memory is addressed by the result of an

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instruction which processes the content of the first memory cell in the variable memory and the further parameters.

In addition, the variable memory is addressed using a first bit length a, and the table memory is addressed using a second bit length b, where the first bit length a and the second bit length b may be of different size.

The invention also relates to an apparatus for carrying out the method, where the program memory is connected to the processor by means of a first bidirectional bus. In addition, an addressing unit is provided which receives first addresses from the processor via a first bus and converts the first addresses into second addresses, and thus uses a second bus to address a variable memory which can be read by the processor via a third bus, and a table memory connected to the processor by means of a second bidirectional bus is provided.

Preferably, a device is provided which receives data from the variable memory via a fourth bus and receives data from the processor via a fifth bus and uses the received data to calculate an address for addressing the variable memory via a sixth bus.

In addition, the variable memory is a read/write memory, and the table memory is preferably in the form of a read/write memory. The processor is preferably in the form of an I/O processor for protocol processing.

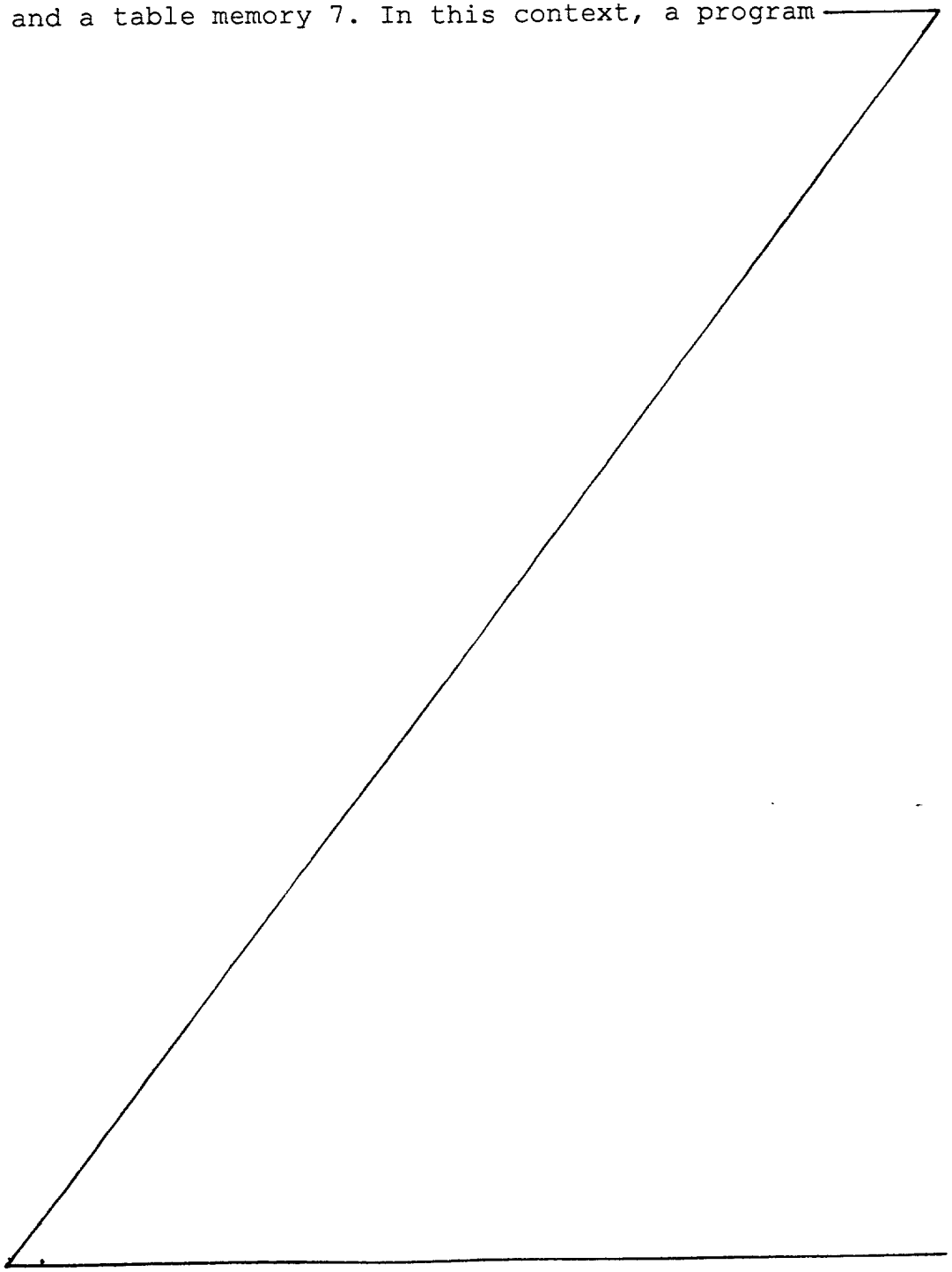
Preferred embodiments of the invention are explained below with reference to the drawings, in which

figure 1 shows an exemplary embodiment of the inventive method, and

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figure 2 shows an exemplary embodiment of the inventive apparatus for carrying out the method.

Figure 1 is a schematic illustration of the inventive method, using a program memory 5, a variable memory 6 and a table memory 7. In this context, a program



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13 in the variable memory 6 has a bit length of b bits. To address the table memory, the content of the register 13 in the variable memory 6 is transferred to the table memory 7 in the form of a second address signal 3. The memory cell addressed in the table memory 7 is then read and loaded into the program counter of the processor.

The new program counter value 14 which is then in the program counter now addresses (third addressing signal 4 having a length of c bits) the memory cell having the address x + y in the program memory, which address indicates the branch destination 15 for the branch operation or jump in the program.

The two-stage execution of the method - first stage: addressing the variable memory 6, second stage: addressing the table memory 7 - allows an indirect branch instruction based on the inventive method to be adjusted to different requirements very flexibly.

The additional option of influencing or varying the addressing of the register 13 in the variable memory using the unit 10 allows the jump or branch destination to be varied as the BRI instruction is executed.

A processor processing the BRI instruction can be prompted to change the branch or jump destination, for example by a data stream which is to be processed. The parameters 11 thus permit the processor to control the unit 10 such that another memory cell or another register in the variable memory 6 is addressed instead of the register 13 in the variable memory 6, which was originally anticipated by the BRI instruction. This means that the jump or branch destination of the BRI instruction can be changed as the first stage of the instruction is actually being executed.

It is also possible for the content of the variable memory 6 to be varied by the processor or by other devices by means of reprogramming 9. This allows the jump or branch destinations of the BRI instructions to be varied. It is therefore possible to react flexibly to further variations in the program flow or in the program execution.

Figure 2 shows an apparatus for carrying out the inventive method. Elements which are already shown in figure 1 are identified using the same reference symbols as in figure 1.

A processor 100 containing a program counter PC can be connected to other devices by means of buses 111 and 112.

The processor 100 uses the program counter PC to address a program memory 5 connected to the processor by means of a bidirectional bus 103.

If the processor 100 encounters a BRI instruction for a program branch operation when executing a program from the program memory, the processor 100 addresses a variable memory 6 via an addressing unit 101. The variable memory 6 in turn contains addresses for addressing a table memory 7.

For this purpose, the addressing unit 101 receives addresses from the processor 100 via a unidirectional bus 104. The addressing unit 101 converts these addresses into addresses for addressing the variable memory 6, said addresses being transmitted from the addressing unit 101 to the variable memory 6 via a unidirectional bus 105. As a result, in the variable memory 6, a memory cell is addressed which contains the address of a further memory cell in the variable memory 6.

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The content of the memory cell in the variable memory 6 is supplied via a unidirectional bus 106 to a unit for address calculation 102.

The unit for address calculation 102 receives from the processor 100 further data via a unidirectional bus 108 and uses the content of the memory cell in the variable memory 6 and the data from the processor to calculate an address for addressing the further memory cell in the variable memory. This address is transmitted from the unit for address calculation 102 to the variable memory 6 via a unidirectional bus 107.

This indirect calculation of an address in the table memory, which in turn contains the addresses of the jump destinations, provides the option of varying the jump destinations on the basis of data which the processor 100 sends to the unit for address calculation 102.

The content of the now-addressed second memory cell in the variable memory 6 is read by the processor via a unidirectional bus 109.

The processor then uses this address to address the table memory 7, which is connected to the processor by means of a bidirectional bus 110. The content of the addressed memory cell in the table memory 7 is read by the processor via the bidirectional bus 110 and is written to the program counter PC.

The program counter PC in turn uses the bidirectional bus 103 to address the program memory at the anticipated jump or branch destination.

The variable memory 6 can additionally be reprogrammed by the processor via a bidirectional bus 113. This

allows the addresses stored in the variable memory to be reprogrammed for addressing the table memory 7.

In addition, the table memory 7 can be reprogrammed by the processor via the bidirectional bus 110. This provides another opportunity for reprogramming all the branch operations or jump destinations of the BRI instructions.

The invention can be used, in particular, in special processors for protocol processing for telecommunication protocols, such as ISDN.

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ART 34 AMD

Patent Claims

1. A method for branching when a program is executed by a processor (100), where the program is stored in a program memory (5), and a variable memory (6) and a table memory (7) for storing fixed values are provided, the processor (100) executing the following steps:

 a) a first memory cell (12) in the variable memory (6) is addressed (1),

 b) a second memory cell (13) in the variable memory is addressed (2) on the basis of the content of the first memory cell (12), addressed in step a), and further parameters (11),

 c) a memory cell (14) in the table memory (7) is addressed (3) on the basis of the content of the second memory cell (13), addressed in step b), and

 d) execution branches to a program address (15) which is stored in that memory cell (14) in the table memory (7) which was addressed in step c).

2. The method as claimed in claim 1, characterized in that, in step b), the second memory cell (13) in the variable memory (6) is addressed by the result of an instruction (10) which processes the content of the first memory cell (12) in the variable memory (6) and further parameters (11).

3. The method as claimed in claim 1 or 2, characterized in that the variable memory (6) is addressed (1) using a first bit length a, and the

table memory (7) is addressed (3) using a second bit length b, the first bit length a and the second bit length b being of different size.

4. An apparatus for carrying out the method as claimed in claim 1, where

the program memory (5) is connected to the processor (100) by means of a bidirectional bus (103),

an addressing unit (101) is provided which receives first addresses from the processor (100) via a bus (104) and converts the first addresses into second addresses, and thus uses a bus (105) to address the variable memory (6), which can be read by the processor (100) via a bus (109), and

the table memory (7) is connected to the processor (100) by means of a bidirectional bus (110).

5. The apparatus as claimed in claim 4, characterized in that a device (102) is provided which receives data from the variable memory (6) via a bus (106) and receives data from the processor (100) via a bus (108), and uses the received data to calculate an address for addressing the variable memory (6) via a bus (107).

6. The apparatus as claimed in claim 4 or 5, characterized in that the variable memory (5) is a read/write memory.

7. The apparatus as claimed in claim 4, 5 or 6, characterized in that the table memory (7) is a read/write memory.

8. The apparatus as claimed in one of Claims 4 to 7, characterized in that the processor (100) is in the form of an I/O processor for protocol processing.

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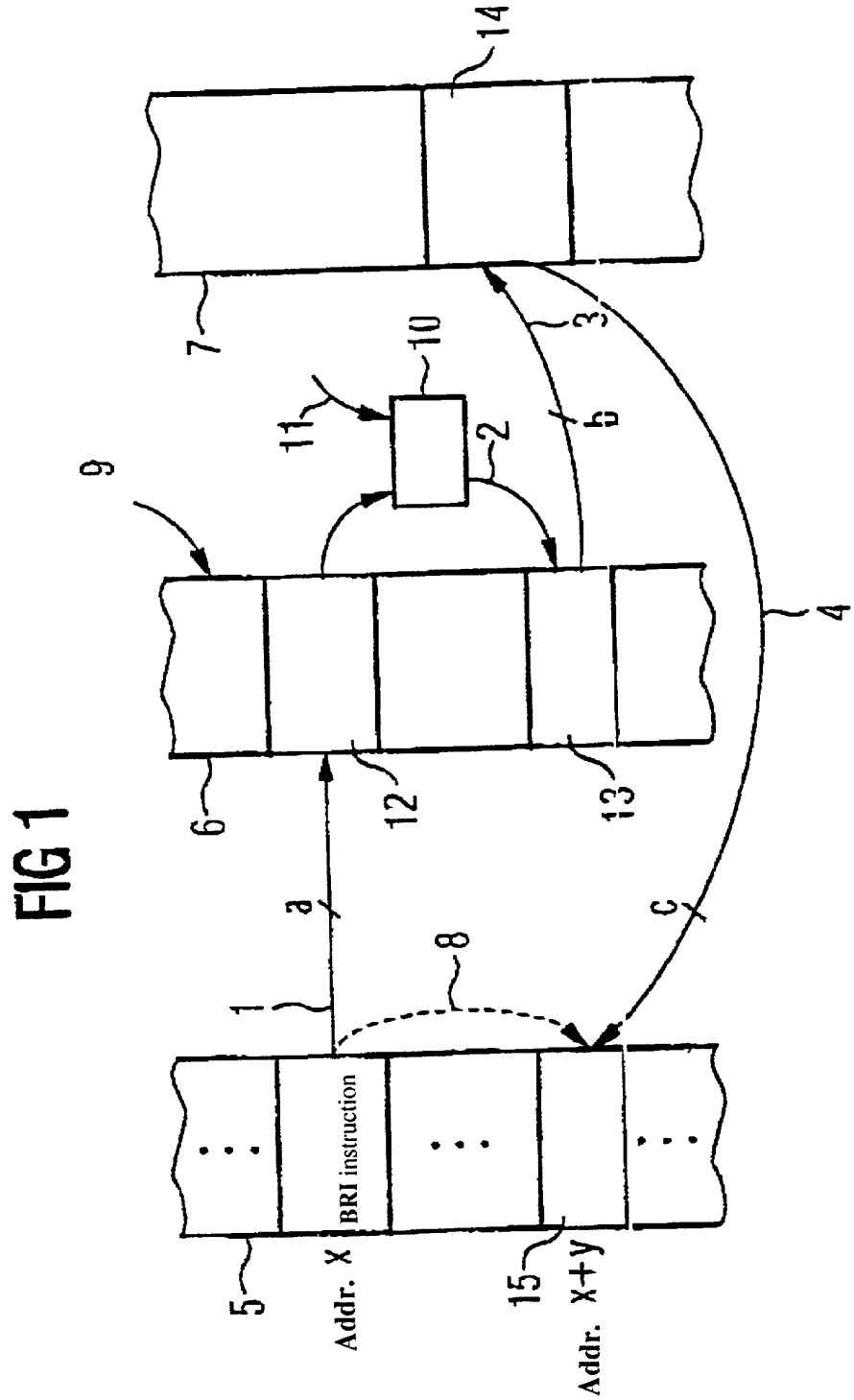
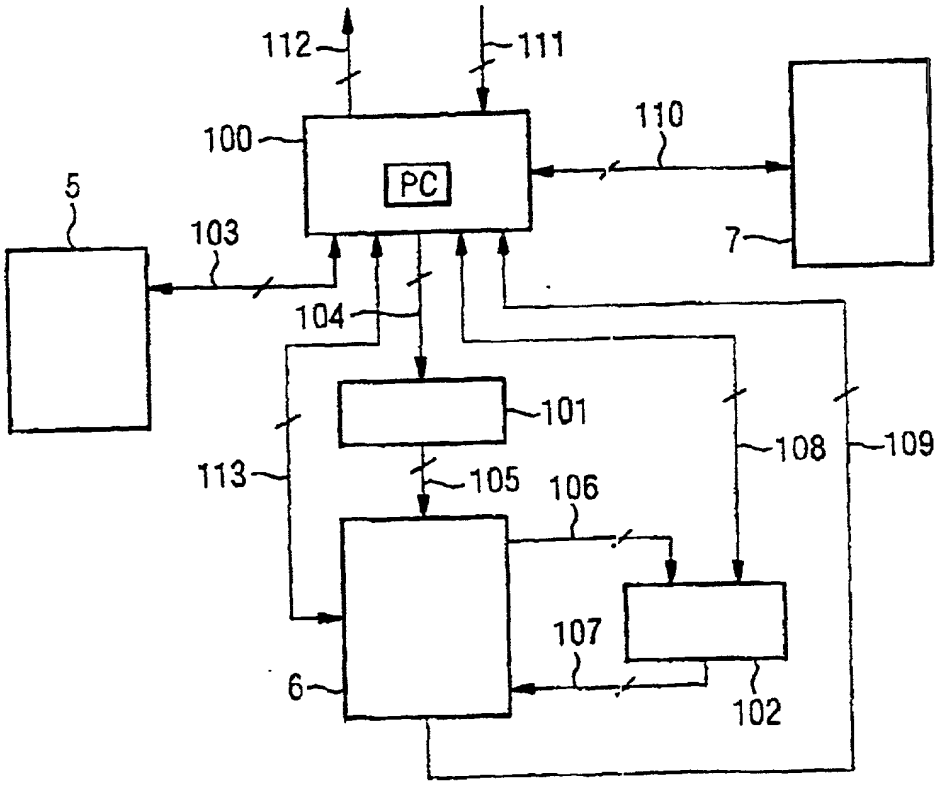


FIG 1

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FIG 2



20020304.4305956

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PTO/SB/01 (10-00)
Approved for use through 10/31/2002 OMB 0651-0032
U S Patent and Trademark Office; U S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

☐ Declaration Submitted with Initial Filing OR ☒ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number	1406/24
First Named Inventor	JENSEN, Karsten
COMPLETE IF KNOWN	
Application Number	09/980,974
Filing Date	October 26, 2001
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, mailing address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD AND DEVICE FOR BRANCHING DURING THE PROCESSING OF A PROGRAM BY A PROCESSOR

(Title of the Invention)

the specification of which

☐ is attached hereto

OR

☒ was filed on (MM/DD/YYYY) 10/26/2001 as United States Application Number or PCT International Application Number 09/980,974 and was amended on (MM/DD/YYYY) _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
199 23 517.1	Germany	05/21/1999	☐	☐	☒
PCT/DE00/01610	WIPO	05/19/2000	☐	☐	☒
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)

☐ Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

Burden Hour Statement. This form is estimated to take 21 minutes to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

JC18 Rec'd PCT/PTO 26 OCT 2001

FORM PTO-1390 (REV. 11-2000) U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: 1406/24

U.S APPLICATION NO. (If known, see 37 CFR 1.5): 09/980974

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE00/01610	19 May 2000 (19.05.00)	21 May 1999 (21.05.99)

TITLE OF INVENTION: METHOD AND DEVICE FOR BRANCHING DURING THE PROCESSING OF A PROGRAM BY A PROCESSOR

APPLICANT(S) FOR DO/EO/US: INFINEON TECHNOLOGIES, AG; JENSEN, Karsten and HOBER, Peter

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [] This is a **SECOND or SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [] This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. [X] The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
 a. [] is attached hereto (required only if not communicated by the International Bureau).
 b. [X] has been communicated by the International Bureau.
 c. [] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [X] An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
 a. [X] is attached hereto.
 b. [] has been previously submitted under 35 U.S.C. 154(d)(4).
7. [X] Amendments to the claims of the International Aplication under PCT Article 19 (35 U.S.C. 371(c)(3))
 a. [] are attached hereto (required only if not communicated by the International Bureau).
 b. [] have been communicated by the International Bureau.
 c. [] have not been made; however, the time limit for making such amendments has NOT expired.
 d. [X] have not been made and will not be made.
8. [] An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. [X] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [X] An English lanugage translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included

11. [] An Information Disclosure Statement under 37 CFR 1.97 and 1
12. [] An assignment document for recording. A separate cover sheet
13. [X] A FIRST preliminary amendment.
14. [] A SECOND or SUBSEQUENT preliminary amendment.
15. [] A substitute specification.
16. [] A change of power of attorney and/or address letter.
17. [] A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. [] A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. [] A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. [X] Other items or information:

Copy of cover page of PCT Publication WO 00/72311; Copy of International Search Report; Copy of International Preliminary Examination Report w/ Annexes (in German)

"Express Mail" mailing label Number EL863524037US
Date of Deposit 26 · 10 · 01
I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231. Katrina T. Holland, Lillian S. Glenn, Amy J. Martin, Karen S. Flynn, Paige E. Snyder, Shaylor E. Dunn.
Paul A. Williams

APPLICATION NO (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
09/980974	PCT/DE00/01610	1406/24

21. [X] The following fees are submitted:

	CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)):		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a (2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1000.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$860.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$710.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$690.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 890.00	
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CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	8 -20 =	0	**x $18.00**	$ 0.00	
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MULTIPLE DEPENDENT CLAIM(S) (if applicable)			**+ $270.00**	$ 0.00	
TOTAL OF ABOVE CALCULATIONS =				$ 890.00	
[] Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				+ $ 0.00	
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c. [X] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-0426. A duplicate copy of this sheet is enclosed.

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NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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PATENT TRADEMARK OFFICE

Richard E. Jenkins
SIGNATURE

Richard E. Jenkins
NAME

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

NAME OF SOLE OR FIRST INVENTOR : [] A petition has been filed for this unsigned inventor

Given Name (first and middle [if any]) FW Karsten | Family Name or Surname Jensen

Inventor's Signature Karsten Jensen | Date 11/15/01

Residence: City Freital | State | Country DE | Citizenship DE

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NAME OF SECOND INVENTOR: [] A petition has been filed for this unsigned inventor

Given Name (first and middle [if any]) Peter | Family Name or Surname Hober

Inventor's Signature | Date

Residence: City Riemerling | State | Country DE | Citizenship DE

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[] Additional inventors are being named on the ___supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto.

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NAME OF SOLE OR FIRST INVENTOR : [] A petition has been filed for this unsigned inventor

Given Name (first and middle [if any]): Karsten | Family Name or Surname: Jensen

Inventor's Signature | Date

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City: Freital | State | ZIP: D-01705 | Country: Germany

NAME OF SECOND INVENTOR: [] A petition has been filed for this unsigned inventor

Given Name (first and middle [if any]): Peter | Family Name or Surname: Hober

Inventor's Signature:  | Date: 11/21/01

Residence: City: Riemerling | State | Country: DE | Citizenship: DE

Mailing Address: Sommerstr. 18

Mailing Address

City: Riemerling | State | ZIP: D-85521 | Country: Germany

[] Additional inventors are being named on the ____supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto.